



Application Note

# Astra™ Machina Foundation Series – UART

Abstract: This document details UART connection to Astra™ Machina Foundation Series evaluation modules containing the SL16xx and SL261x SoCs

Downloaded by anonymous () on 7 Jul 2026 16:36:10 UTC

# Contents

1.	Overview .....	5
1.1.	Scope.....	6
2.	UART (x) Introduction.....	7
2.1.	UART (x) Timing.....	7
2.2.	SL16xx and SL261x UART(x) Baud Rate .....	8
2.2.1.	Baud Rate Calculation .....	8
3.	SL16xx and SL261x UART Pinmux.....	10
4.	SL16xx and SL261x UART Program Flow.....	13
5.	References.....	15
6.	Revision History .....	16

Downloaded by Anonymous () on 7 Jan 2026 16:36:10 UTC

## List of Figures

Figure 1. Astra Machina Foundation Series overview .....	5
Figure 2. UART pins on 40-pin header (J32) Astra Machina IO board.....	6
Figure 3. Serial Data Format.....	7
Figure 4. Receiver Serial Data Sample Points.....	7
Figure 5. Flowchart UART Transmit Programming Example.....	13
Figure 6. Flowchart UART Receive Programming Example .....	14

Downloaded by Anonymous () on 7 Jan 2026 16:36:10 UTC

## List of Tables

Table 1. UART to USB supported Drivers .....	6
Table 2. UART to USB supported Drivers.....	7
Table 3. SL261x and SL16xx UART block Clock Source .....	8
Table 4. UART Baud Rate Configuration Registers .....	9
Table 5. SL1680 UART Pinmux .....	10
Table 6. SL1640 UART Pinmux .....	10
Table 7. SL1620 UART Pinmux.....	11
Table 8. SL261x UART Pinmux.....	12

Downloaded by Anonymous () on 7 Jan 2026 16:36:10 UTC

## 1. Overview

The Astra™ Machina Foundation Series offers evaluation-ready kits that facilitate quick and straightforward prototyping with the Synaptics SL-Series of embedded Linux® and Android™ processors. Featuring a modular design, these kits include interchangeable core compute modules, a standard I/O board, and daughter cards for connectivity, debugging, and various I/O configurations. Additionally, the Astra Machina Foundation Series features UART(x) technology.

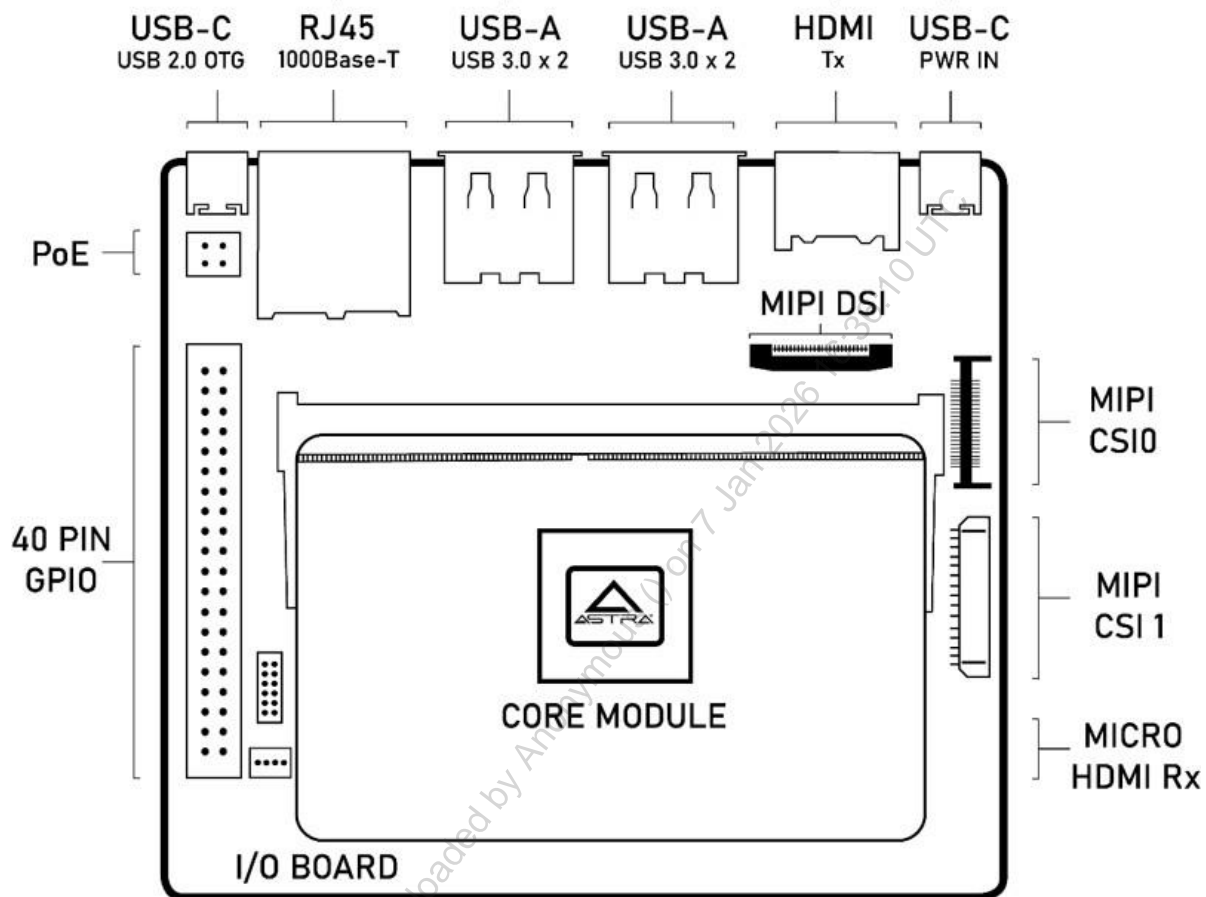


Figure 1. Astra Machina Foundation Series overview

## 1.1. Scope

This document details UART connection to Astra™ Machina Foundation Series evaluation modules containing the SL16xx series and SL261x SoCs. The supported UART to USB debug/console driver IC are listed.

SL1680, SL1640/SL1620			
3.3V	1	2	5.0V
TWO_SDA	3	4	5.0V
TWO_SCL	5	6	GND
PWM[1]	7	8	UART0 Tx
GND	9	10	UART0 Rx
I2S2_BCLK/TW1_SCL	11	12	GPIO10/CM GPIO-EXP 0 2
I2S2_LRCK/TW1_SDA	13	14	GND
I2S2_DI[0]/I2S1_DI	15	16	ADCI[0]/PWM[2]
3.3V	17	18	ADCI[1]/GPIO2
SPI2_SDO	19	20	GND
SPI2_SDI	21	22	GPIO37/GPIO55
SPI2_CLK	23	24	SPI2_SS0n
GND	25	26	SPI2_SS1n
PDMB_CLKIO/PDM_CLKIO	27	28	PDMA_DI[1]/PDM_DI[1]
PDMA_DI[0]/GPIO22	29	30	GND
GPIO39/GPIO48	31	32	GPIO38/GPIO47
GPIO36/CM GPIO-EXP 0 7	33	34	GND
I2S1_LRCK	35	36	SPI2_SS3n
I2S1_MCLK	37	38	I2S1_BCLK
GND	39	40	I2S1_DO[0]/I2S1_DO

SL2610			
3.3V	1	2	5.0V
TW2_SDA	3	4	5.0V
TW2_SCL	5	6	GND
SM_PWM2	7	8	SM_URT0_TX
GND	9	10	SM_URT0_RX
SM_GPIO27	11	12	SM_GPIO34
SM_GPIO26	13	14	GND
I2S2_DI	15	16	ADCI[0]
3.3V	17	18	ADCI[1]
SM_SPI1_SDO	19	20	GND
SM_SPI1_SDI	21	22	GPIO29
SM_SPI1_SCLK	23	24	SM_GPO25
GND	25	26	SM_SPI1_SS3n
SM_PDM_CLKIO	27	28	SM_PDM_DI1
URT4_RXD	29	30	GND
URT4_TXD	31	32	SM_GPIO29
GPIO30	33	34	GND
I2S2_LRCK	35	36	SM_GPIO28
I2S2_MCLK	37	38	I2S2_BCLK
GND	39	40	I2S2_DO

Figure 2. UART pins on 40-pin header (J32) Astra Machina IO board

UART to USB driver modules are connected to 40-pin header (J32) for debug/console.

Table 1. UART to USB supported Drivers

UART to USB driver modules Pin Function	Astra SL16xx/SL261x RDK 40-pin Connector	Astra SL16xx/SL261x RDK 40-pin Function
5V-Out	NC	NC
TX-Out	Pin-10	UART0_Rx-In
RX-IN	Pin-8	UART0_Tx-Out
GND	Pin-6	GND

Supported UART to USB driver modules:

1. Adafruit USB to UART Debug / Console Cable (CP2102 Driver IC)
  - o <https://www.digikey.com/en/products/detail/adafruit-industries-llc/954/7064488>
  - o <https://www.adafruit.com/product/954#technical-details>
  - o [https://item.taobao.com/item.htm?\\_u=e1cfiiqc248&id=37946005623&spm=a1z09.2.0.0.40112e8dTnAnEI&skuld=4878151064465](https://item.taobao.com/item.htm?_u=e1cfiiqc248&id=37946005623&spm=a1z09.2.0.0.40112e8dTnAnEI&skuld=4878151064465)
2. CenryKay USB to UART Debug / Console Cable (CH340G Driver IC)
  - o [https://www.amazon.com/dp/B09Z2GZ6W4?ref=ppx\\_yo2ov\\_dt\\_b\\_product\\_details&th=1](https://www.amazon.com/dp/B09Z2GZ6W4?ref=ppx_yo2ov_dt_b_product_details&th=1)

## 2. UART (x) Introduction

Universal Asynchronous Receiver/Transmitter (UART) is a peripheral device for asynchronous serial communication in which the data format and transmission speeds are configurable.

### 2.1. UART (x) Timing

Table 2. UART to USB supported Drivers

Parameter	Condition	Typ1	Units
TX bit width	±5%	8.68	µs
RX bit width	±5%	8.68	µs

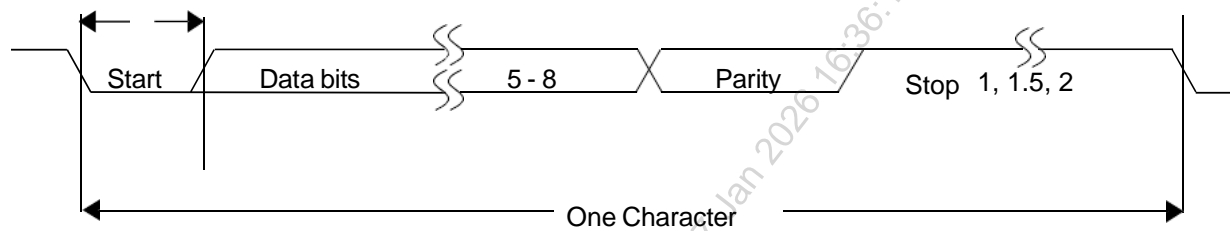


Figure 3. Serial Data Format

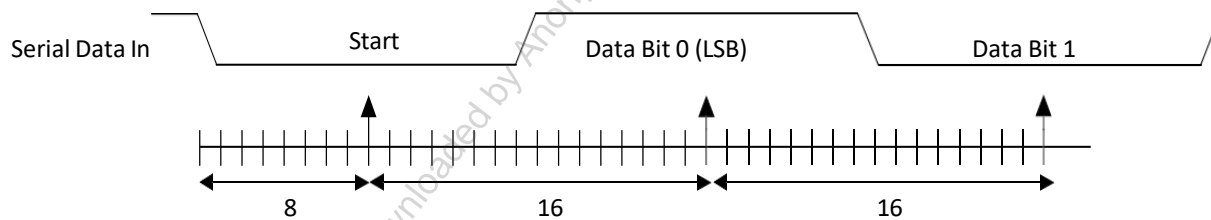


Figure 4. Receiver Serial Data Sample Points

## 2.2. SL16xx and SL261x UART(x) Baud Rate

SL16xx/SL261x Series UART Interface support various Baud Rates. However, SL16xx/ SL261x Series application set and verified at 115.2K Baud.

Table 3. SL261x and SL16xx UART block Clock Source

UART(x)	SL1680 Clk source
SM_UART(0)	25 MHz
SM_UART(1)	25 MHz
SOC_UART(2)	100 MHz
SOC_UART(3)	100 MHz

UART(x)	SL1640 Clk source
SM_UART(0)	25 MHz
SM_UART(1)	25 MHz
SOC_UART(2)	100 MHz

UART(x)	SL1620 Clk source
SOC_UART(1)	100 MHz
SOC_UART(2)	100 MHz

UART(x)	SL261x Clk source
SM_UART(0)	25 MHz
SM_UART(1)	100 MHz
SM_UART(2)	100 MHz
SM_UART(3)	100 MHz
SOC_UART(4)	100 MHz
SOC_UART(5)	100 MHz
SOC_UART(6)	100 MHz
SOC_UART(7)	100 MHz

### 2.2.1. Baud Rate Calculation

#### Divider Mechanism:

To achieve high accuracy and minimal baud deviation, the UART uses a combined integer and fractional divider system. This mechanism allows precise baud generation from reference clocks,

The baud rate clock is calculated as:

$$F_{OUT} = \frac{F_{CLK\_IN}}{16 \times \left( \text{Integer} + \frac{\text{Frac}}{16} \right)}$$

Where:

- F\_OUT is the desired baud rate,
- F\_CLK\_IN is the input clock frequency,
- Integer is the integer divider (from DLL and DLH),
- Frac is the 4-bit fractional component (from DLF).

## Formula to Calculate Dividers

Given a target baud rate:

$$\text{Integer} = \text{Int} \left( \frac{F_{\text{CLK\_IN}}}{16 \times \text{BaudRate}} \right)$$

$$\text{Frac} = \text{Round} \left( 16 \times \left( \frac{F_{\text{CLK\_IN}}}{16 \times \text{BaudRate}} - \text{Integer} \right) \right)$$

## Constraints

- Integer divider must be greater than 2
- Frac must be non-zero
- The resulting baud rate deviation should be < 2%, to meet UART standards.

Table 4. UART Baud Rate Configuration Registers

Register	Offset	Field	Description
DLL	0x00	[7:0]	Divisor Latch Low (Integer part LSB)
DLH	0x04	[7:0]	Divisor Latch High (Integer part MSB)
DLF	0xC0	[3:0]	Divisor Latch Fraction (4-bit Frac)
LCR	0x0C	[7] DLAB	Divisor Latch Access Bit (enable DLL/DLH access)

### 3. SL16xx and SL261x UART Pinmux

Following are the SL261x and SL16xx UART Pinmux tables.

Table 5. SL1680 UART Pinmux

Pin #	Mode 0	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7
AW51	SM_URTO_RXD	–	–	–	–	–	–
AW55	SM_URTO_TXD	–	–	–	–	–	–
AY59	–	–	–	–	–	–	SM_URT1_CTSn
AR55	–	–	–	–	–	M_URT1_RTSn	–
AB60	–	SM_URT1_RXD	–	–	–	–	–
AG59	–	SM_URT1_TXD	–	–	–	–	–
AT59	–	–	–	–	URT2_TXD	–	–
AY59	–	–	–	–	URT2_RXD	–	–
AY60	–	–	URT2_RTSn	–	–	–	–
AY57	–	–	URT2_CTSn	–	–	–	–
W47	–	–	–	URT3_RXD	–	–	–
R51	–	–	–	URT3_TXD	–	–	–
W49	–	–	–	URT3_CTSn	–	–	–
R53	–	–	–	URT3_RTSn	–	–	–

Table 6. SL1640 UART Pinmux

Pin #	Mode 0	Mode 1	Mode 2	Mode 4	Mode 5	Mode 6	Mode 7
AL28	SM_URTO_TXD	–	–	–	–	–	–
AK28	SM_URTO_RXD	–	–	–	–	–	–
AC32	–	SM_URT1_TXD	–	–	–	–	–
AD31	–	SM_URT1_RXD	–	–	–	–	–
AK31	–	–	–	–	–	SM_URT1_RTSn	–
AL30	–	–	–	–	–	–	SM_URT1_CTSn
AK32	–	–	–	–	URT2A_TXD	–	–
AL30	–	–	–	–	URT2A_RXD	–	–
AN30	–	–	URT2A_RTSn	–	–	–	–
AL29	–	–	URT2A_CTSn	–	–	–	–
B5	–	–	–	URT2B_RXD	–	–	–
B6	–	–	–	URT2B_TXD	–	–	–
B7	–	–	–	URT2B_CTSn	–	–	–
A8	–	–	–	URT2B_RTSn	–	–	–

Table 7. SL1620 UART Pinmux

Pin #	Mode 0	Mode 2	Mode 3
F14	URTOA_RXD	—	—
B15	URTOA_TXD	—	—
A8	—	URTOA_CTSn	—
B8	—	URTOA_RTSn	—
B13	—	URTOB_RXD	—
C12	—	URTOB_TXD	—
N31	—	URTOB_CTSn	—
P27	—	URTOB_RTSn	—
C22	—	URT1A_RXD	—
C23	—	URT1A_TXD	—
B21	—	URT1A_RTSn	—
C21	—	URT1A_CTSn	—
B25	—	—	URT1B_TXD
B26	—	—	URT1B_RXD
C26	—	—	URT1B_RTSn
C27	—	—	URT1B_CTSn

Table 8. SL261x UART Pinmux

Pin #	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
V30	—	SM_URTO_TXD	—	—	—	—	—
T30	—	SM_URTO_RXD	—	—	—	—	—
T31	SM_URTO_RXD	—	—	—	—	SM_URT1_RXD	—
U26	SM_URTO_TXD	—	—	—	—	SM_URT1_TXD	—
P29	—	SM_URTO_CTSn	—	—	—	SM_URT1_CTSn	—
P30	—	SM_URTO_RTSn	—	—	—	SM_URT1_RTSn	—
R29	SM_URT1_RXD	—	—	—	—	SM_URTO_RXD	—
N30	SM_URT1_TXD	—	—	—	—	SM_URTO_TXD	—
L29	—	SM_URT2_TXD	—	SM_URT3_RTSn	SM_URT3_DE	—	—
K29	—	SM_URT2_RXD	—	SM_URT3_CTSn	SM_URT3_REn	—	—
J29	—	SM_URT3_TXD	—	SM_URT2_RTSn	SM_URTO_RTSn	—	SM_URT1_RTSn
H30	—	SM_URT3_RXD	—	SM_URT2_CTSn	SM_URTO_CTSn	—	SM_URT1_CTSn
F19	—	SM_URT1_RXD	—	—	SM_URTO_RXD	—	—
A21	—	SM_URT1_TXD	—	—	SM_URTO_TXD	—	—
B21	—	—	SM_URT2_TXD	SM_URT3_RTSn	—	SM_URT3_DE	—
C21	—	—	SM_URT2_RXD	SM_URT3_CTSn	—	SM_URT3_REn	—
F21	—	SM_URT1_RTSn	SM_URT3_TXD	SM_URT2_RTSn	—	SM_URTO_RTSn	—
C22	—	SM_URT1_CTSn	SM_URT3_RXD	SM_URT2_CTSn	—	SM_URTO_CTSn	—
C6	URT5_RXD	—	—	SM_URT1_RXD	—	—	—
C5	URT5_TXD	—	—	SM_URT1_TXD	—	—	—
A3	—	URT4_TXD	—	SM_URT1_RTSn	—	—	—
B2	—	URT4_RXD	—	SM_URT1_CTSn	—	—	—
A6	—	URT4_DE	—	SM_URT1_RXD	—	—	—
B6	—	URT4_Ren	—	SM_URT1_TXD	—	—	—
C9	—	—	—	URT5_RXD	—	—	—
B9	—	—	—	URT5_TXD	—	—	—
D11	—	—	—	URT6_RXD	—	—	—
A9	—	—	—	URT6_TXD	—	—	—
B12	—	—	—	URT7_RXD	—	—	—
C13	—	—	—	URT7_TXD	—	—	—
C14	—	—	—	—	SM_URT1_RTSn	—	—
B14	—	—	—	—	SM_URT1_CTSn	—	—

## 4. SL16xx and SL261x UART Program Flow

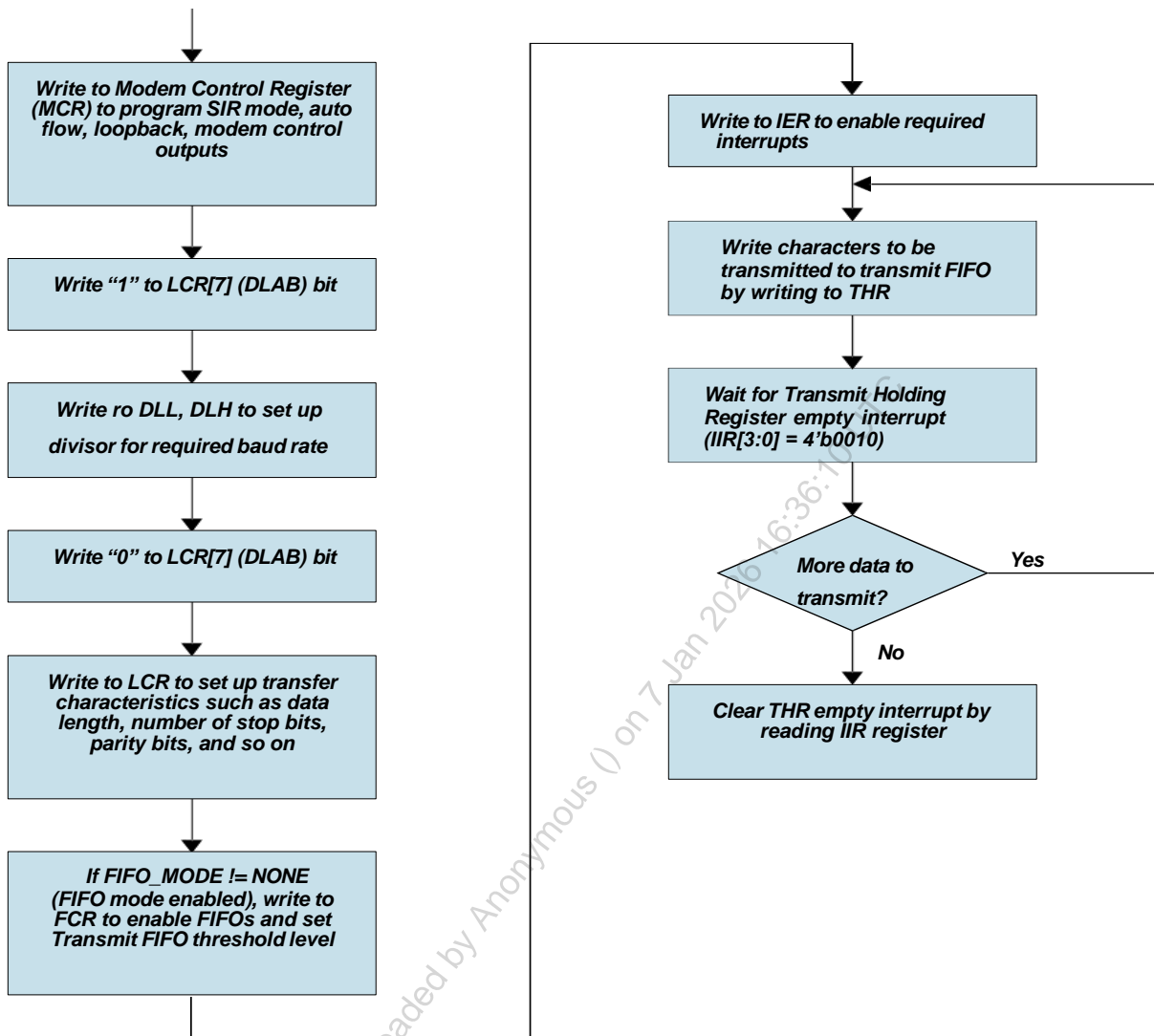


Figure 5. Flowchart UART Transmit Programming Example

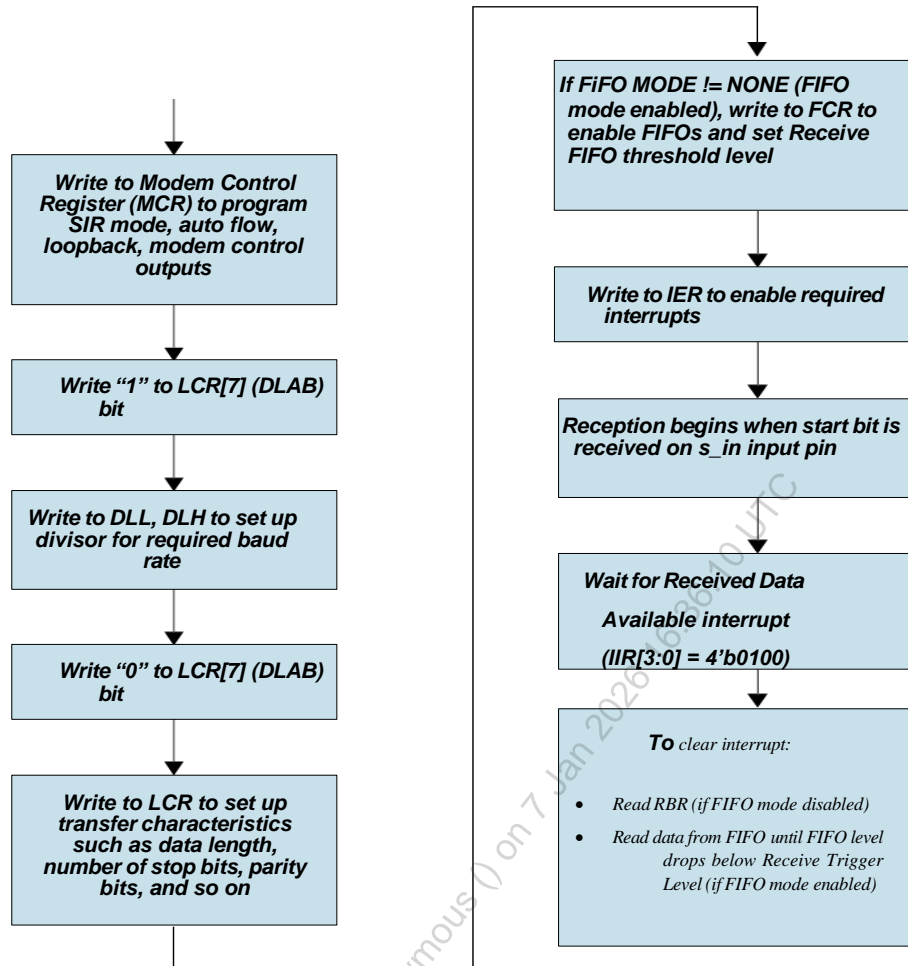


Figure 6. Flowchart UART Receive Programming Example

## 5. References

---

- *Astra Machina Foundation Series Quick Start Guide* (PN: 511-001404-01)
- *Astra Machina SL1640 Developer Kit User Guide* (PN: 511-001405-01)
- *Astra Machina SL1620 Developer Kit User Guide* (PN: 511-001407-01)
- *Astra Machina SL1680 Developer Kit User Guide* (PN: 511-001403-01)
- *Astra Machina SL2600 Series Developer Kit User Guide* (PN: 511-001453-01)

Downloaded by Anonymous () on 7 Jan 2026 16:36:10 UTC

## 6. Revision History

Revision	Description
A	Initial release.
B	Updated Pinmux Table
C	Added SL261x information.

Downloaded by Anonymous () on 7 Jan 2026 16:36:10 UTC



### Copyright

Copyright © 2024–2025 Synaptics Incorporated. All Rights Reserved.

### Trademarks

Synaptics, the Synaptics logo, Astra Machina, and the Astra logo are trademarks or registered trademarks of Synaptics Incorporated in the United States and/or other countries.

Android is a trademark of Google LLC. Linux is the registered trademark of Linus Torvalds in the U.S. and other countries. All other trademarks are the properties of their respective owners.

### Contact Us

Visit our website at [www.synaptics.com](http://www.synaptics.com) to locate the Synaptics office nearest you.

PN: 506-001506-01 Rev C

### Notice

Use of the materials may require a license of intellectual property from a third party or from Synaptics. This document conveys no express or implied licenses to any intellectual property rights belonging to Synaptics or any other party. Synaptics may, from time to time and at its sole option, update the information contained in this document without notice.

INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED "AS-IS," AND SYNAPTICS HEREBY DISCLAIMS ALL EXPRESS OR IMPLIED WARRANTIES, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND ANY WARRANTIES OF NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT SHALL SYNAPTICS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES ARISING OUT OF OR IN CONNECTION WITH THE USE OF THE INFORMATION CONTAINED IN THIS DOCUMENT, HOWEVER CAUSED AND BASED ON ANY THEORY OF LIABILITY, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, AND EVEN IF SYNAPTICS WAS ADVISED OF THE POSSIBILITY OF SUCH DAMAGE. IF A TRIBUNAL OF COMPETENT JURISDICTION DOES NOT PERMIT THE DISCLAIMER OF DIRECT DAMAGES OR ANY OTHER DAMAGES, SYNAPTICS' TOTAL CUMULATIVE LIABILITY TO ANY PARTY SHALL NOT EXCEED ONE HUNDRED U.S. DOLLARS.